What is claimed is:

1. A digital image processing device comprising:

a signal processing unit to process a video input signal;

a frame memory to store a result from the processing performed by said signal processing unit; and

a redundant pixel embedding circuit to embed a redundant pixel not to be displayed in an image line read from said frame memory and to produce a video output signal.

2. The digital image processing device according to Claim 1, wherein said redundant pixel embedding circuit has a function of receiving, as an input, an image line read from said frame memory and of embedding, according to an embedding control signal fed from outside, a redundant pixel in a specified position in said image line.

3. A digital image processing device comprising:

a signal processing unit to process a video input signal;

a frame memory to store a result from the processing performed by said signal processing unit;

a serial-parallel converting circuit to receive image data read from said frame memory in a time-series manner and to produce an output making up an image line,

a redundant pixel embedding circuit to embed a redundant pixel not to be displayed in said image line and to output data, and

a parallel-serial converting circuit to output said image

line in which said redundant pixel is embedded as time-series image data.

4. The digital image processing device according to Claim 3, wherein said serial-parallel converting circuit which is made up of a register file being able to store an image line and which has a function of sequentially storing image data fed from said frame memory in a time-series manner according to a writing control signal fed from outside and of reading, simultaneously and in parallel, contents of all registers in said register file.

5. The digital image processing device according to Claim 3, wherein said redundant pixel embedding circuit has a function of receiving, as an input, said image line read from said serial-parallel converting circuit and of embedding, according to an embedding control signal fed from outside, a redundant pixel in a specified position in said image line.

6. The digital image processing device according to Claim 3, wherein said parallel-serial converting circuit has a register file made up of two or more shift registers and a selector to select an output from each of said shift registers and to output the selected output and wherein said register file is able to store an image line in one clock cycle and wherein each of said shift registers is able to perform a shifting operation, according to a reading control signal fed from outside, in synchronization with a clock signal and wherein said selector has a function of selecting a specified shift output from said shift register and of outputting the selected output according to an embedding

control signal fed from outside.

7. The digital image processing device according to Claim 6, wherein each of said shift registers is made up of two or more split shift registers and wherein each of said split shift registers receives a data input, shift data input, latch signal input, and shift signal input and produces a shift data output and wherein each of said shift registers has a function of writing, when data is to be written to said split shift registers, data at one time, by making active a latch signal input, in synchronization with a clock and, at time of shifting operations, of performing said shifting operation for data, by making active a shift signal input, in synchronization with a clock and of feeding a shift output fed from each of said split shift registers to said selector by connecting a terminal for a shift output from each of said split shift registers to a terminal for a shift input of each of adjacent split shift registers to allow said shift register to perform said shift operation as a whole.

8. A digital image processing device comprising:

a signal processing means to process a video input signal;

a frame memory to store a result from the processing performed by said signal processing means; and

a redundant pixel embedding means to embed a redundant pixel not to be displayed in an image line read from said frame memory and to produce a video output signal.

9. The digital image processing device according to Claim 8, wherein said redundant pixel embedding means has a function of

receiving, as an input, an image line read from said frame memory and of embedding, according to an embedding control signal fed from outside, a redundant pixel in a specified position in said image line.

10. A digital image processing device comprising:

a signal processing means to process a video input signal;

a frame memory to store a result from the processing performed by said signal processing means;

a serial-parallel converting means to receive image data read from said frame memory in a time-series manner and to produce an output making up an image line,

a redundant pixel embedding means to embed a redundant pixel not to be displayed in said image line and to output data, and

a parallel-serial converting means to output said image line in which said redundant pixel is embedded as time-series image data.

11. The digital image processing device according to Claim 10, wherein said serial-parallel converting means which is made up of a register file being able to store an image line and which has a function of sequentially storing image data fed from said frame memory in a time-series manner according to a writing control signal fed from outside and of reading, simultaneously and in parallel, contents of all registers in said register file.

12. The digital image processing device according to Claim 10, wherein said redundant pixel embedding means has a function of receiving, as an input, an image line read from said serial-

parallel converting means and of embedding, according to an embedding control signal fed from outside, a redundant pixel in a specified position in said image line.

13. The digital image processing device according to Claim 10, wherein said parallel-serial converting means has a register file made up of two or more shift registers and a selector to select an output from each of said shift registers and to output the selected output and wherein said register file is able to store an image line in one clock cycle and wherein each of said shift registers is able to perform a shifting operation, according to a reading control signal fed from outside, in synchronization with a clock signal and wherein said selector has a function of selecting a specified shift output from said shift register and of outputting the selected output according to an embedding control signal fed from outside.

14. The digital image processing device according to Claim 13, wherein each of said shift registers is made up of two or more split shift registers and wherein each of said split shift registers receives a data input, shift data input, latch signal input, and shift signal input and produces a shift data output and wherein each of said shift registers has a function of writing, when data is to be written to said split shift registers, data at one time, by making active a latch signal input, in synchronization with a clock and, at time of shifting operations, of performing said shifting operation for data, by making active a shift signal input, in synchronization with a clock and of feeding a shift output fed from each of said split shift registers

to said selector by connecting a terminal for a shift output from each of said split shift registers to a terminal for a shift input of each of adjacent split shift registers to allow said shift register to perform said shift operation as a whole.